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TRANSIENT VOLTAGE PROTECTION FOR SOLID STATE CONTROLS

Any device that uses power semiconductors to control AC power can by damaged by transient voltage spikes on the AC line. Caused by electrical activity elsewhere in the power system, these spikes last only nanoseconds, but their magnitude may be great enough to destroy semiconductors. Manufacturers of solid state motor starters and SCR controls, therefore, always include some type of protection against transient spike damage in their product designs.

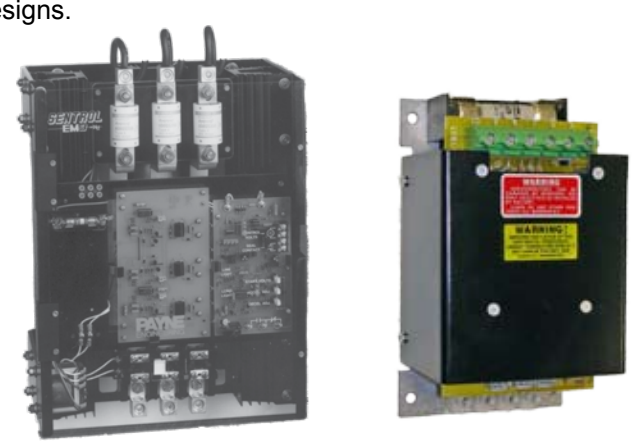

Figure 1. Solid state motor starter (left), SCR power control

SCRs and diodes are both unidirectional semiconductors: they conduct voltage from anode to cathode, and block voltage from cathode to anode. When a transient voltage spike exceeds the cathode to anode blocking capability, known ad Peak Inverse Voltage (PIV) rating, that semiconductor will fail shorted, similar to a welded contact in an electromechanical contactor. Power Company studies show that such voltage spikes are common occurrences, and their magnitudes are neither predictable nor limited. The long-term reliability of any solid state control, therefore, is directly dependent on the effectiveness of the transient voltage protection incorporated in its design.

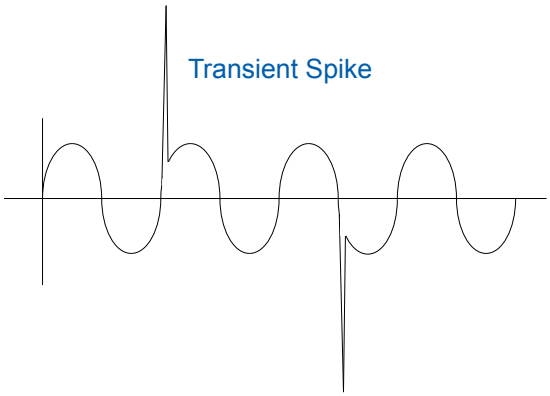

Figure 2. Transient voltage spikes on a typical AC waveform

Transient voltage protection methods can be grouped into three general categories:

a. Selecting the PIV rating of the semiconductors to withstand transients without being damaged;

b. Using a suppression mechanism to shunt transients around semiconductors;

c. Self-protection, utilizing an SCR characteristic to prevent destructive inverse voltages from being impressed on the semiconductors.

A. Peak Inverse Voltage Ratings

This method of transient protection is the simplest, and at the same time the most limited, SCRs and diodes are selected to have a certain minimum PIV rating, which is “guess-timated” to be sufficient to allow them to withstand the transient spikes to which they may be subjected. Since there is no way to predict the magnitude of transient spikes that may be encounter, there is no sure way to select a PIV rating other than pure guesswork. Is 1000 PIV enough? 1200? 2000? Quite simply, there is no way to know.

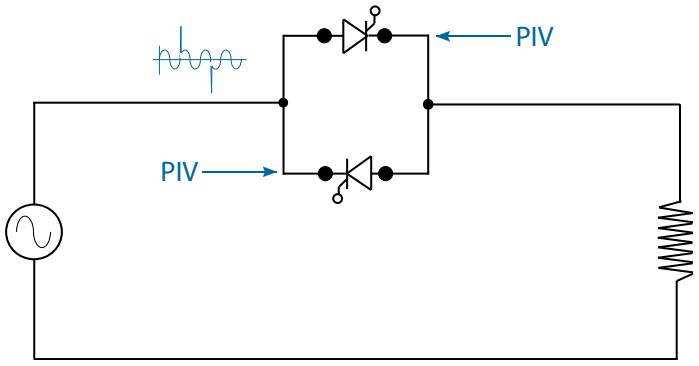

Figure 3. Inverse-parallel SCRs utilizing PIV ratings for transient spike protection

Transient voltage spikes 3kV or greater are not uncommon on industrial power mains, while the PIV ratings on power semiconductors range from 600 to perhaps 2000 V. Clearly, positive transient protection requires more than just the selection of a discrete PIV rating in the power semiconductors.

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B. Suppression

Suppression schemes incorporate metal oxide varistors (MOVs) to shunt transient spikes around blocking semiconductors to limit the inverse voltage impressed on them. MOVs are bi-directional solid state switches that block voltage until their threshold level is reached, at which time they switch to a conducting state and remain there as long as the applied voltage stays above that threshold. Connected in parallel to and inverse parallel pair of power semiconductors, and selected for a turn-on threshold below semiconductor PIV ratings, MOVs will limit the inverse voltage levels impressed on those semiconductors.

The limiting factor to any suppression scheme is the total energy rating of the MOVs used to shunt the transient spikes. The greater the spike magnitude, the grater the energy content, so the greater the MOV energy rating must be to handle it. Should that rating ever be exceeded, MOVs fail--sometimes literally exploding--leaving the semiconductors unprotected against the next transient event. So, what energy rating is required? Since there is no way to predict spike magnitudes, the energy rating selection process is pure guesswork. No matter what value is finally selected, a spike with a higher energy content is not only possible, but likely.

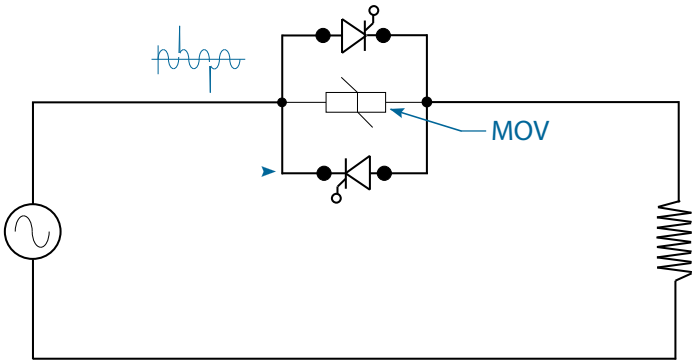

Figure 4. MOV connected to shunt spikes around inverse-parallel pair of SCR's

C. Self-Protection

The greatest degree of transient voltage protection is afforded by utilization of a non-destructive forward turn-on characteristic of all SCRs known as Voltage Breakover (Vbo). When a forward-blocking SCR is subjected to a high-enough forward voltage, it will "break over" -- turn on-- without being commanded to do so by control circuitry. Proper coordination of the Vbo and PIV ratings on an inverse-parallel pair of

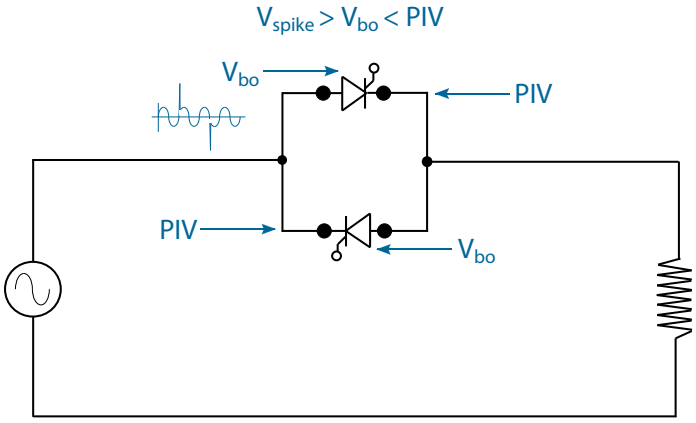

Figure 5. Inverse-parallel SCRs selected for V_{bo} Clamping

SCRs will ensure that, in the event of a transient voltage spike that exceeds a certain level, the forward-facing device will turn on non-destructively to shunt the spike around the reverse-facing one before the latter's PIV level is reached. This method is known as Vbo Clamping.

Vbo Clamping ensures that the inverse voltages impressed on a semiconductor will never exceed a pre-determined level, and that the semiconductors themselves carry the full energy of a shunted transient spike. Protection against system-generated transient spikes is insured, regardless of PIV ratings.

Summary:

The reliability and long term viability of a solid state control in an industrial environment is in large measure determined by the effectiveness of the transient voltage protection incorporated into its design. The methods used are:

a. PIV ratings: semiconductors are selected for their high reverse-blocking capability. The problem: how high is high? PIV ratings range from 600 to 2000 volts; regardless of the PIV selected, there's a good chance a higher transient will be encountered.

b. MOVs: transients are shunted around semiconductors so destructive inverse voltages are not impressed on them. The problem: is a high-magnitude spike exceeds the MOV energy rating, it will fail, eliminating all transient protection. Selection of MOV energy ratings is pure guesswork, since there is no way to predict spike magnitudes.

c. Voltage Breakover: forward turn-on characteristic of SCRs is coordinated with PIV ratings to cap the maximum inverse voltage impressed on semiconductors below destructive levels at spike magnitudes at greater than PIV ratings. Positive, repeatable, protection against any normal system-generated spikes is provided.